Discipline	DESIGNING WITH PROGRAMMABLE LOGIC code: 46/47/48 - 7 **summer semester**	
Specialty	Computer Science and Technologies	
ECTS credits: **6**	Form of assessment: exam	
Lecturer	Assoc. Prof. Slava Yordanova, PhD Room Phone: +359 52 383 E-mail: slava_y@tu-varna.bg	
Department	Computer Science and Engineering	
Faculty	Faculty of Computing and Automation	

Learning objectives:

The course: Designing with Programmable Logic, is taught by students in semester 8. It uses Altera FPGA kits and learns and uses a language to design electronic circuits - Verilog. Various electronic devices (triggers, registers, adders, multiplexers, processors, etc.) are synthesized and a Verilog algorithm and program for their simulation is created using kits. The material is distributed in 30 hours of lectures and 30 hours of exercises.

Exercises are performed on models, and the simulation is on a computer, for this purpose hall 513-1E is equipped.

CONTENTS:

Training Area	Hours lectures	Hours seminar exercises
FPGA - principles of action	4	4
Design language for Verilog electronic circuits	8	8
Finite State Machines	8	8
Design of processors	10	10
TOTAL: 60 h	**30**	**30**